

Remarks

The non-final Office Action dated June 17, 2009, lists the following rejections: claims 1-3 and 15-18 stand rejected under 35 U.S.C. § 103(a) over Yamada (U.S. Patent No. 5,757,639) in view of Stancil (U.S. Patent No. 6,272,584); and claim 14 stands rejected under 35 U.S.C. § 103(a) over the '639 reference in view of the '584 reference and further in view of May (U.S. Patent No. 7,343,483). In the following discussion, Applicant does not acquiesce in any regard to averments in this Office Action (unless Applicant expressly indicates otherwise).

Embodiments of Applicant's invention relate to the use of (existing) test circuitry (e.g., JTAG-compliant circuitry) for the purpose of communicating data from an external memory, such as loading programming instructions or code images. Accordingly, Applicant has introduced amendments toward such embodiments.

Applicant respectfully traverses the § 103(a) rejections because the cited combination of references lacks correspondence. Regarding claim 1, the references fail to teach or suggest using test circuitry that provides debugging capabilities to also communicate data such as programming instructions between the ICs. Regarding claim 10, the references fail to teach or suggest using test circuitry for providing debugging functionality to also communicate program code. Regarding claim 15, the references fail to teach or suggest test circuits that are configured to communicate both debugging information and code images, in respective modes.

Applicant notes that the addition of the '483 reference does not cure the above-mentioned deficiencies. Although the '483 reference mentions JTAG, it neither teaches nor suggests the above-mentioned aspects (e.g., the use of JTAG to transfer code images to a processor). As explained in M.P.E.P. § 2143, "(t)he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." As JTAG circuitry is not taught to be used in the manner claimed nor is there any suggestion toward this end in the references, the rejection cannot stand and there is not a *prima facie* case of obviousness.

In view of the above, Applicant believes that each of the rejections is improper and should be withdrawn and that the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilska, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 
Name: Robert J. Crawford
Reg. No.: 32,122
Shane O. Sondreal
Reg. No.: 60,145
651-686-6633
(NXPS.633PA)